IN THE CLAIMS

Following are the claims as amended and currently pending for consideration:

1-15. (Cancelled)

16. (Currently Amended) A processor comprising:

a decode unit to decode a plurality of packed data instructions including a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, and a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction and to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction, said second set of operations including at least multiplying corresponding packed data elements of the second set of packed data to produce products and summing said products by pairs; and

an execution unit to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit.

17. (Cancelled)

18. (Previously Presented) The processor of Claim 16, wherein the first set of operations comprises:

a packed subtract and write carry (PSBWC) operation;

a packed absolute value and read carry (PABSRC) operation; and

a packed add horizontal (PADDH) operation.

19-20. (Cancelled)

21. (Previously Presented) The processor of Claim 16, wherein performing the first operation causes the execution unit to:

produce a first plurality of partial products in a multiplier having a plurality of partial product selectors;

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit.

22. (Previously Presented) The processor of Claim 21, wherein performing the first operation further causes the execution unit to:

shift the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result.

23. (Previously Presented) A processor comprising:

a decode unit to decode a plurality of packed data instructions including a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, and a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction and to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction; and

an execution unit to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit;

wherein performing the first operation causes the execution unit to:

produce a first plurality of partial products in a multiplier having a plurality of partial product selectors,

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions, and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit;

and wherein performing the second operation causes the execution unit to:

produce a second plurality of partial products in the multiplier having the plurality of partial product selectors, the second plurality of partial products comprising four distinct sets of partial products including a first set of partial products

corresponding to a first product for elements of the second set of packed data, a second set of partial products corresponding to a second product for elements of the second set of packed data, a third set of partial products corresponding to a third product for elements of the second set of packed data, and a fourth set of partial products corresponding to a fourth product for elements of the second set of packed data, and

add the first set of partial products together with the second set of partial products to produce a first distinct element of a packed result and add the third set of partial products together with the fourth set of partial products to produce a second distinct element of the packed result.

24. (Previously Presented) The processor of Claim 23, wherein the second format identifies the second set of packed data as packed words.

25-38. (Cancelled)

39. (Currently Amended) A processor comprising:

decode logic to decode a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, said decode logic to generate a microcode sequence responsive to decoding the PSAD instruction to initiate a first set of operations on the first set of packed data ~~responsive to decoding the PSAD instruction~~, the first set of operations comprising:

a packed subtract and write carry (PSUBWC) operation;

a packed absolute value and read carry (PABSRC) operation; and

a packed add horizontal (PADDH) operation.; and

execution logic to perform the first set of operations initiated by the decode logic.

40. (Previously Presented) The processor of Claim 39, wherein the first format identifies the first set of packed data as packed bytes.

41. (Previously Presented) The processor of Claim 39, wherein performing the PSUBWC operation causes the execution logic to:

subtract one of a plurality of elements of a first packed data of the first set of packed data from a corresponding one of a plurality of elements of a second packed data of the first set of packed data to produce a first result having a plurality of difference elements and a plurality of sign indicators; and

store the plurality of difference elements and the plurality of sign indicators.

42. (Previously Presented) The processor of Claim 39, wherein performing the PABSRC operation causes the execution logic to:

receive a plurality of difference elements and a plurality of sign indicators;

produce a result data having a plurality of absolute value elements, each absolute value element produced by

(a) subtracting one of the plurality of difference elements from a corresponding constant value if the sign indicator corresponding to that element is in a first state, or

(b) adding one of the plurality of difference elements to a corresponding constant value if the sign indicator corresponding to that element is in a second state.

43. (Previously Presented) The processor of Claim 39, wherein performing the PADDH operation causes the execution logic to:

produce a first plurality of partial products in a multiplier having a plurality of partial product selectors;

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit.

44. (Previously Presented) The processor of Claim 43, wherein performing the PADDH operation further causes the execution logic to:

shift the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result.